maintaining a link between addresses of any unusable memory cell blocks and addresses of substitute usable memory cell blocks,

in response to a write request from a host system, initially writing new data intended for the EEprom memory cell array into a cache memory instead of the EEprom memory cell array,

thereafter, in response to additional space for new data being required in the cache memory, directing at least a portion of the data stored in the cache memory to be written into the EEprom memory cell array with an address including at least one of said memory cell blocks, and

writing said at least a portion of the data stored in the cache memory into the EEprom memory cell array by a method including:

if said at least one of said memory cell blocks is usable, writing said at least a portion of the data stored in the cache memory into said at least one of said memory cell blocks, and

if said at least one of said memory cell blocks is unusable, writing said at least a portion of the data stored in the cache memory into at least one of the substitute usable memory cell blocks that is linked with said at least one of said memory cell blocks.

64. The method of claim 63, wherein said at least a portion of the data stored in the cache memory that is written into the EEprom memory cell array includes that which has been stored in the cache memory for the longest time.

65. The method of claim 63, wherein the individual blocks of memory cells are operated with both user data and overhead data stored therein in non-overlapping portions of the individual blocks.

66. The method of claim 65, wherein overhead data stored in the individual blocks of memory include a characteristic of the individual block in which the user data and overhead data are stored.

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67. The method of claim 65, wherein overhead data stored in the individual blocks of memory includes an error correction code for the user data stored in the same blocks.

68. The method of claim 65, wherein overhead data stored in the individual blocks of memory include an address corresponding to the block in which the overhead data are stored.

69. The method of claim 63, wherein writing at least a portion of the data stored in the cache memory into the EEprom memory cell array includes programming individual memory cells of the EEprom memory cell array into exactly two states in order to store exactly one bit of data per cell.

70. The method of claim 63, wherein writing at least a portion of the data stored in the cache memory into the EEprom memory cell array includes programming individual memory cells of the flash EEprom system into more than two states in order to store more than one bit of data per cell.

71. A method of a host system utilizing a mass data storage system to store data files, said mass data storage system including an array of non-volatile EEprom memory cells partitioned into a plurality of blocks that individually include a distinct group of memory cells that are erasable together as a unit, comprising:

writing individual new data files from the host to a cache memory provided as part of the mass data storage system without writing the new data files to the memory cell array,

when written into the cache memory, reading a data file requested by the host system from the cache memory rather than from the memory cell array,

thereafter writing a selected data file from the cache memory into the memory cell array, said writing including selecting at least one usable memory cell block into which the data file is written that includes either (a) the memory cell block whose address is mapped from a mass storage system address received from the host system, or (b) if the memory cell block whose address is mapped from the received mass storage system address is not useful, another memory cell block that is useful,

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when written into the memory cell array, reading a data file requested by the host system from the memory cell array rather than from the cache memory.

72. The method of claim 71, wherein the individual new data files are written into a volatile random-access-memory as the cache memory.

73. The method of claim 71, wherein the individual new data files are written into a memory separate from the flash EEprom system as the cache memory.

74. The method of claim 71, wherein the mass data storage system is provided on a card that is electrically and mechanically removably connectable with the host computing system.

75. The method of claim 74, wherein the mass data storage system provides an ATA interface with the host computing system.

76. The method of claim 71, wherein selecting a data file and writing the selected data file to the EEprom memory cell array is caused to occur when additional space for new data files is required in the cache memory.

77. The method of claim 71, wherein the data file selected to be written into the memory cell array is selected based upon a length of time since the data file was last written into the cache memory.

78. The method of claim 71, wherein writing a new data file to the cache memory from the host occurs in less time than if written directly into the EEprom memory cell array from the host.

79. The method of claim 71, wherein the individual blocks of memory cells are operated with both user data and overhead data stored therein in non-overlapping portions of the individual blocks.

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80. A bulk storage memory system that is connectable to a host system, said memory system comprising:

an array of non-volatile memory cells arranged to store in designated blocks thereof a given amount of user data and associated overhead data,

a cache memory separate from said non-volatile memory cell array, and

a controller connectable to said host system for controlling operation of the non-volatile memory cell array and the cache memory, said controller including:

an erasing circuit that causes all of the memory cells of one or more designated blocks of the array to be erased together,

an addressing circuit responsive to receipt of a mass memory storage block address from the host system to generate an address of at least one corresponding array block, the addressing circuit being responsive to a list of array blocks that have other array blocks substituted therefore to substitute at least one address of such other array blocks for the generated address of said at least one array,

a first data transfer circuit responsive to the addressing circuit to execute an instruction from the host system to perform a designated one of (1) a data write operation by writing user data to the cache memory, or (2) a data read operation by reading addressed user data first from the cache memory, if stored therein, or from the array, if not stored in the cache memory, and

a second data transfer circuit that removes data from the cache by writing said removed data into the memory array.

81. The memory system according to claim 80, wherein the second data transfer circuit removes data from the cache in response to additional space for new data being required in the cache memory.

82. The memory system according to claim 80, wherein the second data transfer circuit removes data from the cache that has been stored in the cache memory for a time longer than the remaining data therein.

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83. The memory system according to claim 80, wherein the list of array blocks that have other array blocks substituted therefore includes inoperable or defective blocks.

84. The memory system according to claim 83, wherein the inoperable or defective blocks include blocks that contain a number of defective cells in excess of a preset number.

85. The memory system according to claim 80, wherein said given amount of user data is 512 bytes.

86. The memory system according to claim 80, wherein said bulk storage memory system is implemented in a single package that is removably connectable to the host system through an electrical connector.

87. The memory system according to claim 80, wherein the overhead data stored in an individual one of the memory cell array blocks includes an error correction code of the user data stored in said individual block.

88. The memory system according to claim 80, wherein the first and second data transfer circuits write data into the memory cell array with exactly two programmable states per memory cell storage element, thereby to store exactly one bit of data per storage element.

89. The memory system according to claim 80, wherein the first and second data transfer circuits write data into the memory cell array with more than two programmable states per memory cell storage element, thereby to store more than one bit of data per storage element.

90. A method of operating a memory system with a host system, wherein the memory system includes an array of non-volatile memory cells partitioned into a plurality of sectors that individually include a distinct group of memory cells that are erasable together as a unit, comprising:

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providing said memory cell array and a memory controller within a card that is removably connectable to the host system, said controller being connectable to the host system for controlling operation of the memory system when the card is connected thereto,

operating the memory cells within the individual sectors with at least a user data portion and an overhead portion,

detecting a predefined condition when individual sectors become unusable and linking the addresses of such unusable sectors with addresses of other sectors that are useable,

causing the controller, in response to receipt from the host system of an address in a format designating at least one mass memory storage block, to generate an address of a non-volatile memory sector that corresponds to said at least one mass memory storage block,

accessing a usable sector of the memory system, if the sector with the generated address is unusable, by referring to the linked address of another sector that is usable and then accessing that other sector,

either writing data to, or reading data from, the user data portion of the accessed usable sector, and

either writing to, or reading from, said overhead portion of the accessed usable sector, information related to either the accessed usable sector or data stored in the user data portion of said accessed useful sector.

91. The method according to claim 90, wherein the detecting of the predefined condition includes detecting when individual sectors become defective.

92. The method according to claim 91, wherein the detecting of when individual sectors become defective includes determining when a number of individual defective memory cells within a sector exceed a given number.

93. The method according to claim 90, wherein the user data portion of the individual non-volatile memory sectors has a capacity of 512 bytes.

94. The method according to claim 90, wherein the information stored in the overhead portion of the individual sectors includes an address of the respective ones of the individual sectors.

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95. The method according to claim 90, wherein the information stored in the overhead portion of the individual sectors includes an error correction code calculated from data stored in the user data portions of corresponding ones of the individual sectors.

96. The method according to claim 90 wherein linking the address of unusable sectors with sectors that are useable includes maintaining a list within the card that links such unusable sectors with addresses of corresponding ones of the other sectors that are useable, and wherein accessing a usable sector includes referring to the list to translate the address of the unusable sector into an address of a usable sector.

97. The method according to claim 90 wherein linking the address of such unusable sectors includes storing within individual ones of the defective sectors addresses of corresponding useable sectors, and wherein accessing a usable sector corresponding to an unusable sector includes referring to the useable sector address stored in the unusable sector.

98. The method according to claim 90, wherein causing the controller to generate an address of a non-volatile memory sector includes doing so for a non-volatile memory sector that corresponds to only one mass memory storage block, wherein the user data portion of the individual non-volatile memory sectors has a capacity that is substantially the same as a user data portion of said one mass memory storage block.

99. A method of operating a memory system with a host system, wherein the memory system includes an array of non-volatile memory cells partitioned into a plurality of sectors that individually include a distinct group of memory cells that are erasable together as a unit, comprising:

providing said memory cell array and a memory controller within a card that is removably connectable to the host system, said controller being connectable to the host system for controlling operation of the memory system when the card is connected thereto,

operating the memory cells within the individual sectors with at least a user data portion and an overhead portion,

causing the controller, in response to receipt from the host system of an address in a format designating at least one mass memory storage block, to designate an

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address of at least one non-volatile memory sector that corresponds with said at least one mass memory storage block,

either writing user data to, or reading user data from, the user data portion of said at least one non-volatile memory sector, and

either writing to, or reading from, said overhead portion of said at least one non-volatile memory sector, overhead data related either to said at least one non-volatile memory sector or to data stored in the user data portion of said at least one non-volatile memory sector.

100. The method of claim 99, wherein the user data portion of the individual sectors has a capacity of 512 bytes.

101. The method of claim 99, wherein the overhead data stored in said overhead portion of the individual sectors includes addresses of the individual sectors.

102. The method of claim 99, wherein partitioning the memory cells includes partitioning said memory cells within the individual sectors to include an additional portion of spare memory cells.

103. The method of claim 102, wherein the overhead data stored in said overhead portion of the individual sectors includes an identification of any defective cells within the user data portion of corresponding ones of said sectors, said method additionally comprising causing the controller to read the identification of defective cells from the overhead portion of said addressed at least one non-volatile memory sector and then to substitute therefore other cells within the spare cell portion of the addressed at least one non-volatile memory sector.

104. The method of claim 99, additionally comprising causing the controller to identify and store addresses of any defective non-volatile memory sectors within the array, and, wherein designating an address of a sector includes, in response to designating an address of a defective sector, substituting an address of another sector instead.

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105. The method of claim 99, wherein the individual sectors include only one user data portion and only one overhead data portion.

106. The method of claim 99, wherein writing to the accessed usable sector includes programming the individual memory cells thereof into one of exactly two programmable states in order to store exactly one bit of data or information per cell.

107. The method of claim 99, wherein writing to the accessed usable sector includes programming the individual memory cells thereof into one of more than two programmable states in order to store more than one bit of data or information per cell.

108. The method of claim 99, wherein the address of said at least one mass memory storage block is an address of at least one magnetic disk sector.

109. The method of claim 99, wherein communication of mass memory storage block addresses and user data with the controller is in parallel over a bus.

110. A method of operating, with a host system, a non-volatile memory system that includes an array of non-volatile memory cells partitioned into sectors of memory cells that are erasable together as a unit, comprising:

providing said memory array and a memory controller within a card that is removably connectable to the host system, the controller being connectable to said host system for controlling operation of the memory array when the card is connected to the host system, and storage elements of the memory cells within said memory array being individually programmable into one of more than two distinct threshold level ranges corresponding to more than one bit of data per storage element,

causing the controller, in response to receipt from the host system of an address in a format designating at least one mass memory storage sector, to designate an address of at least one non-volatile memory sector that corresponds with said at least one mass memory storage block,

either writing user data to, or reading user data from, said at least one non-volatile memory sector,

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either writing to, or reading from, said at least one non-volatile memory sector, overhead data related either to said at least one non-volatile memory sector or to user data stored in said at least one non-volatile memory sector, and

wherein the writing of user and overhead data includes programming the storage elements of the individual memory cells of the array into said one of more than two distinct threshold level ranges.

111. The method of claim 110, wherein the overhead data written into said at least one non-volatile memory sector includes overhead data generated within the memory controller.

112. The method of claim 110, wherein the user data written into the individual sectors is substantially 512 bytes.

113. The method of claim 110, wherein the overhead data stored in said overhead portion of the individual sectors includes addresses of the individual sectors.

114. The method of claim 113, wherein the overhead data stored in said overhead portion of the individual sectors additionally includes, in those sectors that are defective, addresses of sectors being substituted therefor.

115. The method of claim 110, additionally comprising causing the controller to identify and store addresses of any defective non-volatile memory sectors within the array, and, wherein designating an address of said at least one memory sector includes, in response to designating an address of a defective sector, substituting an address of another sector instead.

116. The method of claim 110, wherein the address of said at least one mass memory storage block includes an address of at least one magnetic disk sector.

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117. The method of claim 110, further comprising erasing data from a selected at least one of the individual sectors of memory cells by simultaneously applying an erase voltage to all of the memory cells within said selected at least one sector, thereby to

simultaneously erase any user data and associated overhead data contained in said at least one sector.

118. The method of claim 117, wherein the memory array cells individually include erase gates, and the erase voltage is simultaneously applied to the erase gates of said selected at least one sector of memory cells.

119. The method of claim 110, wherein the memory cell storage elements are conductive floating gates.--

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